Application No. 09/612,067
Filing Date: 07/07/2000
Attorney Docket No. 73081

Applicant(s): NAUMANN
Examiner: Tri H. PHAN
Group Art Unit: 2616

Amendments to the Claims:

Status of Claims:

Claims 1, 3, 5-10, 13-18, 20-24 are pending for examination.

Claims 2, 4, 11, 12, and 19 were previously canceled.

Claim 1 is amended herein.

Claim 3 is cancelled herein.

Claims 1, 10 and 18 are in independent form.

Claims Listing

1.   (Currently Amended) ~~In a communications system having a router, said router having a PCI-compliant front card, said front card being configured to accept a LAN or WAN-compliant back card, a method for detecting the absence of a Phy Layer device on the back card and communicating said absence to the front card, said~~ A method comprising:

receiving, by a switching input of a tri-state buffer provided on ~~the~~ a PCI-compliant front card comprising an FE MAC in a router, a sensing signal from ~~the~~ a back card comprising an FE Phy in the router, where the tri-state buffer is serially disposed on a IDSEL line corresponding to a particular channel;

if ~~the~~said sensing signal is a logical low, then coupling a IDSEL signal corresponding to a particular channel of ~~the~~said back card to ~~the~~said front card; and

if ~~the~~said sensing signal is not low, then decoupling ~~the~~said IDSEL signal from ~~the~~said front card and providing a logical low signal in the place of ~~the~~said IDSEL signal

~~line, wherein~~

~~said front card comprises an FE MAC, and said back card comprises an FE Phy.~~

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2.   (Canceled)

3.   (Cancelled) The method of claim 1, wherein said tri-state buffer further has an input and an output, said input and output being serially disposed on a IDSEL line corresponding to a particular channel.

4.   (Canceled)

5.   (Previously presented) The method of claim 1, wherein said front card and said back card are coupled via an MII bus.

6.   (Previously presented) The method of claim 1, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 frame/line interface.

7.   (Previously presented) The method of claim 6, wherein said from card and said back card are coupled via a TDM bus.

8.   (Previously presented) The method of claim 1, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

9.   (Previously presented) The method of claim 8, wherein said front card and said back card are coupled via a Utopia bus.

10.   (Previously presented) In a communications system having a router, said router having a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card, an apparatus for detecting the absence of a Phy

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Layer device on the back card and communicating said absence to the front card, said apparatus comprising:

means for switching disposed on the front card comprising a tri-state buffer wherein said tri-state buffer has an input, an output, and a switching input wherein said input and said output of said tri-state buffer being serially disposed on said front card and said switching input of said tri-state buffer is configured to be coupled to said back card, wherein said front card comprises an FE MAC, and said back card comprises an FE Phy;

said means for switching being configured to receive a sensing signal from the back card, said sensing signal having a first and second state;

said means for switching being further configured to provide a predetermined signal to said front card responsive to said state of sensing signal.

11.   (Canceled)

12.   (Canceled)

13.   (Currently amended) The apparatus of claim 10, wherein said from card and said back card are coupled via an MII bus.

14.   (Original) The apparatus of claim 10, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 frame/line interface.

15.   (Original) The apparatus of claim 14, wherein said front card and said back card are coupled via a TDM bus.

16.   (Original) The apparatus of claim 10, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

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17.   (Original) The apparatus of claim 16, wherein said front card and said back card are coupled via a Utopia bus.

18.   (Previously presented) An apparatus for detecting the absence of a LAN or WAN compliant device, said apparatus comprising:

a PCI-compliant front card, said front card being configured to accept a LAN or WAN compliant back card wherein said front card comprises an FE MAC, and said back card comprises an FE Phy;

said front card further having a switch, said switch being a tri-state-buffer being serially disposed on a IDSEL connection corresponding to a particular channel on said front card, said switch being further configured to receive a sensing signal corresponding to said channel from said device by switching input of said tri-state buffer; and

wherein said apparatus is configured to couple said IDSEL connection to said front card if said sensing signal is in a first state, and provide a low potential to said, front card if said sensing signal is in a second state.

19.   (Canceled)

20.   (Original) The apparatus of claim 18, wherein said front card and said back card are coupled via an MII bus.

21.   (Original) The apparatus of claim 20, wherein said front card comprises an HDLC control, and said back card comprises a T1/E1 frame/line interface.

22.   (Original) The apparatus of claim 18, wherein said front card and said back card are coupled via a TDM bus.

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23.   (Previously presented) The apparatus of claim 20, wherein said front card comprises an ATM SAR, and said back card comprises an ATM Phy.

24.   (Original) The apparatus of claim 18, wherein said from card and said back card are coupled via a Utopia bus.